

REMARKS

Reconsideration is respectfully requested.

Claim 1 has been amended for clarification to more precisely recite the insulating interlayer to differentiate the following recitation to “insulating layers”.

The presently pending Claims 1-3, 5, 6 and 8-9 have been rejected under 35 U.S. C. §103(a) over the applicants’ description of the prior art (“AAPA”), as set forth and illustrated in Fig. 2 of this application, in view of Maniar et al.

Applicants continue to respectfully submit that the AAPA does not teach the claimed invention, as is explained in the specification pages 1-6, and in view of the arguments made below. Moreover, neither do Maniar et al. provide any teaching that either together with or separately from AAPA is there any combination that can support the rejection.

Applicants submit the following as background information. General CMP processes remove material from uneven topography on a wafer surface until a flat (planarized) surface is created. This enables film layers to be built up with minimal height variations (for further explanation, the Examiner is invited to see internet web site, <http://www.appliedmaterials.com/products/aboutcmpprocess.html>). This is what the conventional CMP process exactly intends, and AAPA shows such a conventional CMP process together with the disclosure of “the conventional CMP completely planarizes an entire surface regardless of the field and active areas **h** and **t** along a dotted line AA”. That is, according to the conventional method of AAPA, the tops of the gates are non-linear before the patterned dummy gate polysilicon elements are subjected to the CMP process. However, the tops of the gates become linear after the CMP process, because of said planarization effect of the conventional CMP process.

In addition, the specification relating to prior art Fig. 2 of the present application described certain problems generated from a method of forming a gate in a semiconductor device using a conventional process, and suggests that the CMP process be carried out along the dotted line AA'. Further, as explained below, in the conventional method, the CMP process is carried out non-selectively between the insulating interlayer and the dummy gate polysilicon layer. Therefore, upon considering such a planarization effect and non-selective polishing of the conventional CMP process, it is well understood that a linear top profile of metal gates is formed from the conventional method in accordance with the prior art shown in Fig. 2.

Therefore, the Examiner's indication that AAPA includes a method of forming a gate having a non-linear top profile is apparently based on an apparent misunderstanding of the conventional CMP process.

Moreover, according to the present invention, polishing between the insulating layer and the dummy gate polysilicon layer and between the insulating interlayer and the gate metal layer is selectively carried out, more particularly, the polishing selection ratios of the insulating interlayer to the dummy gate polysilicon layer and of the gate metal layer to insulating interlayer are high, particularly over 20 and 50, respectively. This contrasts directly with the teaching of Maniar et al., wherein it is described that "A polishing step should have a selectivity as close to 1:1 (polishing rate of the AB3 layer to the polishing rate of the insulating layer) as possible because of AB3's expected resistance to attack by many chemicals. (...) Because a relatively non-selective polishing method would be used, the abrasive particles will usually be alumina or cerium dioxide" (emphasis added) (see column 5, lines 53-63 of the Maniar et al. reference). Therefore, it is impossible to find in the

teachings of Maniar et al. any motivation or incentive to select the high polishing selection ratios as described in Claim 1 of the present invention, and the Examiner's indication of "the recited selection ratios would be obtained in the process of the combination" (page 4, last line of Detailed Action) is not only not taught, but in fact taught against by Maniar et al.

Overall, according to the present claimed method, metal gates having a non-linear (wave-like) top profile are produced, which solves the problems caused by a method of forming a gate using a conventional process (see column 2, paragraph 18). Use of this method achieves favorable effects, such as reduction of height of the dummy gate polysilicon layer thereby, and the insulating layer being deposited between the gates without voids due to the short dummy gate, etc. (see columns 5-6, numbered paragraphs 45-46 of the published application).

With respect to the indication made in the rejection of Claims 1 and 8 that the "wave-like" profile is inherently shown in the AAPA, Fig. 2, it is respectfully suggested that the "wave-like" profile cannot be formed due to the use in a conventional process, such as that shown in Figs. 1 and 2, of a conventional CMP process on the insulation interlayer 7, see page 4, lines 12-14, which process produces complete planarization of the entire surface along the line AA', as shown in Fig. 2 and as described above. It is important to appreciate that because of the conventional selection ratio being below 1, see page 12, lines 2-4, the CMP polishes all of the surface, so as to result in a completely planarized surface, along the line A-A'; see page 5, lines 13-15, where it is described as: "A general CMP process completely planarizes an entire surface regardless of the field and active areas **h** and **t** along a dotted line AA". Thus, the AAPA illustrated in Fig. 2 cannot but have a linear or "flat" top profile. See page 5, lines 13-15. Accordingly, the indication in the Office Action that the

AAPA describes the “wave-like” profile results from an apparent misunderstanding of the invention, as described and claimed, and thus, the rejection is considered improper.

In view of the above, moreover, the suggestion made in the rejection that it would be obvious to combine the teaching of Maniar et al. as teaching a CMP process using high etch selectivity does not provide the requisite teaching of using such a high selectivity etch in the process described in the Admitted Prior Art.

Therefore the present invention as claimed in Claim 1 is non-obvious over AAPA in view of the lack of teaching of US Patent No. 5,356,833 to Maniar et al. Claims 2-3, 5-6 and 8-9, because of their dependency on Claim 1, are also considered to be patentable.

As a separate and distinct ground indicative of the non-obviousness of the claimed invention, it is respectfully submitted that there exists no disclosure, teaching or suggestion to combine the teachings of the Admitted Prior Art or in the Maniar et al. reference, absent the motivation provided by the invention as disclosed by the inventor herein. See ACS Hospital Syst. Inc. v. Montefiore Hospital, 732 F2d 1572, 1577, 221 USPQ 929, 933 (CAFC 1984). In re Jones, 958 F.2d 347, 21 USPQ2d 1941 (Fed.Cir. 1992).

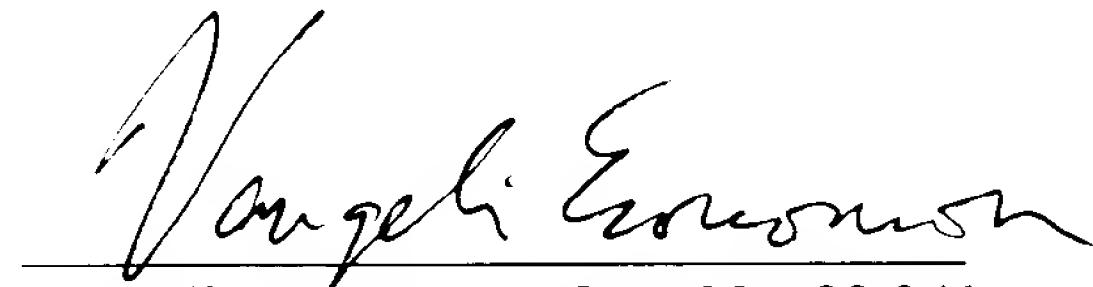
This failure of a suggestion or teaching to combine is even more apparent in light of the teaching away by Maniar et al. from such a combination and also described with respect to the description of the AAPA. As described, the conventional process utilizing a selectivity ratio of less than 1, see above discussion, indicates that the desired result following the completion of the process is a surface having complete planarization.

The present invention is characterized in that the surface polished by CMP has the “wave-like” profile or a non-linear top profile as recited in Claim 1. The rejection asserts that it is an “inherent” result that a CMP process of an insulating interlayer on the topology

of Fig. 2 would result in "a wave-like profile that would be inherently formed." Applicants respectfully suggest that the AAPA teaches the exact opposite of such a result, see page 5, lines 13-15, and that the teachings of Maniar et al fail to provide any guidance toward a high selectivity ratio. The improvement over the prior art itself, argued at pages 1-6 of the specification, is said to be "obvious" based on an inherent result that the AAPA and Maniar et al. both teach against. It is respectfully suggested that this rejection is improperly based on unsupported evidence that is not found in the specification of this application, and therefore a *prima facie* case of obviousness has not been set forth in the rejection. Applicants respectfully request withdrawal of this rejection.

For the above reasons, Applicants respectfully request reconsideration and withdrawal of the outstanding rejections. An indication of allowable subject matter is earnestly solicited.

Respectfully submitted,



Vangelis Economou -Reg. No. 32,341
c/o Ladas & Parry
224 South Michigan Avenue - Suite 1200
Chicago Illinois 60604
Tel. No. (312) 427-1300

July 17, 2003